CLAIMS

1. A non-volatile semiconductor device comprising:

a memory cell array having electrically erasable programmable non-volatile memory cells;

a plurality of reprogramming and retrieval circuits that temporarily store data to be programmed in the memory cell array and sense data retrieved from the memory cell array, each reprogramming and retrieval circuit having a first latch and a second latch, the first latch being connected to a selected bit line of the memory cell array via a first transfer switch and a second transfer switch series-connected to each other, the second latch being connected to a connection node of the first and the second transfer switches via a third transfer switch, a data node of the second latch being connected to data input and output lines via column selection switches; and

a controller that controls the reprogramming and retrieval circuits on data-reprogramming operation to and data-retrieval operation from the memory cell array.

2. The non-volatile semiconductor device according to claim 1, wherein, after the data has been programmed in a selected memory cell, the programmed data is retrieved for programming verification, the retrieved data being sensed and stored in the first latch.

3. The non-volatile semiconductor device according to claim 1, wherein each reprogramming and retrieval circuit has a multilevel logical operation mode and a caching operation mode, in the multilevel logical operation mode, re-programming and retrieval of upper and lower bits of two-bit four-level data being performed using the first and the second latches in storing the two-bit four-level data in one of the memory cells in a predetermined

threshold level range, in the caching operation mode, data transfer between one of the memory cells selected in accordance with a first address and the first latch being performed while data transfer is being performed between the second latch and input/output terminals in accordance with a second address with respect to one-bit two-level data to be stored in one of the memory cells.

4. The non-volatile semiconductor device according to claim 3, wherein in the multilevel logical operation mode, the first and the third transfer switches are turned on to connect the second latch to a selected bit line for pre-charging data stored in the second latch on the bit line.

5. The non-volatile semiconductor device according to claim 3, wherein the four-level data is defined as "11", "10", "00" and "01" from lower level of the threshold level range.

6. The non-volatile semiconductor device according to claim 3, wherein different row addresses are allocated to the upper and the lower bits of the four-level data for programming and retrieval.

7. The non-volatile semiconductor device according to claim 6, wherein a first and a second data programming operation are performed in the multilevel logical operation mode, in the first data programming operation, the lower-bit data being loaded into the second latch and then stored in the first latch, programming being performed to a selected memory cell based on the data stored in the first latch, in the second data programming operation, the upper-bit data being loaded into the second latch and then stored in the first latch while lower-bit data already programmed in the selected memory cell is being retrieved and loaded

into the second latch, programming being performed to the selected memory cell based on the data stored in the first latch in accordance with the data stored in the second latch.

8. The non-volatile semiconductor device according to claim 6, wherein a first, a second and a third retrieval operation are performed in the multilevel logical operation mode, in the first retrieval operation, "0" or "1" of the upper bit being judged using a retrieval voltage applied at a control gate of a selected memory cell, the retrieval voltage being set in a threshold level range of "10" and "00" as the four-level data, in the second retrieval operation, "0" or "1" of the lower bit when the upper bit is "0" being judged using a retrieval voltage applied at the control gate of the selected memory cell, the retrieval voltage being set in a threshold level range of "00" and "01" as the four-level data, and in the third retrieval operation, "0" or "1" of the lower bit when the upper bit is "1" being judged using a retrieval voltage applied at the control gate of the selected memory cell, the retrieval voltage being set in a threshold level range of "11" and "10" as the four-level data.

9. The non-volatile semiconductor device according to claim 1, wherein each reprogramming and retrieval circuit is selectively connected to a plurality of bit lines of the memory cell array via a bit line selection switch.

10. The non-volatile semiconductor device according to claim 1, wherein each reprogramming and retrieval circuit has a common signal line connected to the connection node of the first and the second transfer switches via a fourth transfer switch.

11. The non-volatile semiconductor device according to claim 10, wherein each reprogramming and retrieval circuit has a temporal storing node for temporarily storing a

potential at a data node of the first latch and a fifth transfer switch provided between the fourth transfer switch and the common signal line, the fifth transfer switch being controlled by the potential at the temporal storing node.

12. A non-volatile semiconductor device comprising:

a memory cell array having electrically erasable programmable non-volatile memory cells;

a plurality of reprogramming and retrieval circuits that temporarily store data to be programmed in the memory cell array and sense data retrieved from the memory cell array, each reprogramming and retrieval circuit having a first latch and a second latch that are selectively connected to the memory cell array and transfer data each other; and

a controller that controls the reprogramming and retrieval circuits on data-reprogramming operation to and data-retrieval operation from the memory cell array,

wherein each reprogramming and retrieval circuit has a caching operation mode in which data transfer between one of the memory cells selected in accordance with a first address and the first latch being performed while data transfer is being performed between the second latch and input and output terminals in accordance with a second address with respect to two-level data to be stored in one of the memory cells.

13. The non-volatile semiconductor device according to claim 1, wherein a data programming cycle for a selected memory cell of the memory cell array is performed by repeatedly programming pulse application and retrieval for programming verification, in a test mode, a cell current flowing in the selected memory cell is retrieved to the input and output terminals while the data programming cycle is interrupted during which the data

retrieved by the retrieval for programming verification is stored in the first latch and the second latch is inactive.

14. The non-volatile semiconductor device according to claim 12, wherein a data programming cycle for a selected memory cell of the memory cell array is performed by repeatedly programming pulse application and retrieval for programming verification, in a test mode, a cell current flowing in the selected memory cell is retrieved to the input and output terminals while the data programming cycle is interrupted during which the data retrieved by the retrieval for programming verification is stored in the first latch and the second latch is inactive.

15. A non-volatile semiconductor device comprising:

a memory cell array having electrically erasable programmable non-volatile memory cells;

a plurality of reprogramming and retrieval circuits that temporarily store data to be programmed in the memory cell array and sense data retrieved from the memory cell array; and

a controller that controls the reprogramming and retrieval circuits on data-reprogramming operation to and data-retrieval operation from the memory cell array,

wherein each reprogramming and retrieval circuit includes:

a first transistor provided between a sense node and a selected bit line of the memory cell array;

a second transistor having a gate connected to the sense node and a source to which a reference potential is applied, for detecting a potential level of the sense node;

a first latch connected to a drain of the second transistor via a third transistor that is selectively turned on;

a second latch connected to the drain of the second transistor via a fourth transistor that is selectively turned on and also connected to data input and output lines via a selection gate circuit;

a fifth transistor for selectively connecting the first latch to the selected bit line of the memory cell array and

a sixth transistor for selectively connecting the second latch to the sense node.

16. The non-volatile semiconductor device according to claim 15 wherein each reprogramming and retrieval circuit has a multilevel logical operation mode and a caching operation mode, in the multilevel logical operation mode, re-programming and retrieval of upper and lower bits of two-bit four-level data being performed using the first and the second latches in storing the two-bit four-level data in one of the memory cells in a predetermined threshold level range, in the caching operation mode, data transfer between one of the memory cells selected in accordance with a first address and the first latch being performed while data transfer is being performed between the second latch and input and output terminals in accordance with a second address with respect to one-bit two-level data to be stored in one of the memory cells.

17. The non-volatile semiconductor device according to claim 16 wherein, in the multilevel logical operation mode, the first and the sixth transistors are turned on to pre-charge the selected bit line using the data stored in the second latch for retrieval for programming verification.

18. The non-volatile semiconductor device according to claim 15 further comprising a capacitor, a first terminal thereof being connected to the sense node, the capacitor controlling a potential at the sense node with a second terminal as a drive terminal.

19. A non-volatile semiconductor device comprising:

a memory cell array having non-volatile memory cells, data being stored in a selected non-volatile memory cell in accordance with existence of a current flowing through the selected cell or a level of the current; and

a sense amplifier circuit for retrieving the data on a selected bit line, the sense amplifier circuit including:

a sense node connected to the selected bit line via a clamp transistor;

a pre-charging circuit for pre-charging the bit line via the clamp transistor connected to the sense node;

an inverter having an input terminal connected to the sense node via transfer transistor; and

a boosting capacitor, a first terminal thereof being connected to the sense node, the capacitor boosting a potential at the sense node using a second terminal as a drive terminal.

20. The non-volatile semiconductor device according to claim 19, wherein the sense amplifier circuit pre-charges the bit line through the pre-charging circuit while the clamp transistor is being turned on, continuously pre-charging the sense node while the clamp transistor is being turned off and pre-charging circuit is being turned on during which a potential on the pre-charged bit line varies in accordance with data stored in a selected non-volatile memory cell, turns off the pre-charging circuit to drive the boosting capacitor, while applying a first potential to the drive terminal, to boost the potential at the sense node,

and applies a retrieval voltage to a gate of the clamp transistor to transfer the data on the bit line to the sense node.

21. The non-volatile semiconductor device according to claim 20, wherein the sense amplifier circuit continuously lowers the retrieval voltage to a level higher than a threshold level of the clamp transistor and then stops boosting the sense node by applying a second potential to the drive terminal of the boosting capacitor, the second potential being lower than the first potential.

22. The non-volatile semiconductor device according to claim 19 further comprising an auxiliary capacitor having a first terminal connected to the sense node, and a second terminal being supplied with a reference potential.

23. The non-volatile semiconductor device according to claim 19, wherein the transfer transistor is driven by a gate voltage required for pre-charging the input terminal of the inverter to a voltage which is higher than the threshold voltage of the inverter, while the data on the bit line is being sensed.

24. The non-volatile semiconductor device according to claim 19 further comprising:

an auxiliary capacitor having a first terminal connected to the input terminal of the inverter, and a second terminal being supplied with a reference potential; and

an auxiliary pre-charging circuit for pre-charging the input terminal of the inverter to a power supply voltage.

25. The non-volatile semiconductor device according to claim 19, wherein the inverter is included in a latch for storing the retrieved data.

26. A non-volatile semiconductor device comprising:

a memory cell array having non-volatile memory cells, data being stored in a selected non-volatile memory cell in accordance with existence of a current flowing through the selected cell or a level of the current; and

a sense amplifier circuit for retrieving the data on a selected bit line, the sense amplifier circuit including:

a sense node connected to the selected bit line via a clamp transistor;

a pre-charging circuit for pre-charging the bit line via the clamp transistor connected to the sense node;

an inverter having an input terminal connected to the sense node via transfer transistor;

a first capacitor having a first terminal connected to the sense node, and a second terminal being supplied with a reference potential; and

a second capacitor having a first terminal connected to the input terminal of the latch, and a second terminal being supplied with the reference potential.

27. A non-volatile semiconductor device comprising:

a memory cell array having non-volatile memory cells, data being stored in a selected non-volatile memory cell in accordance with existence of a current flowing through the selected cell or a level of the current; and

a sense amplifier circuit for retrieving the data on a selected bit line, the sense amplifier circuit including:

a sense node connected to the selected bit line via a clamp transistor;

a pre-charging circuit for pre-charging the bit line via the clamp transistor connected to the sense node;

a sense transistor, a source thereof being supplied with a reference potential;

a latch having a data node connected to a drain of the sense transistor via transfer transistor; and

a boosting capacitor, one of two terminals thereof being connected to the sense node, the capacitor boosting a potential at the sense node using the other terminal as a drive terminal.

28. The non-volatile semiconductor device according to claim 27, wherein the sense amplifier circuit pre-charges the bit line through the pre-charging circuit while the clamp transistor is being turned on, continuously pre-charging the sense node while the clamp transistor is being turned off and the pre-charging circuit is being turned on during which a potential on the pre-charged bit line is varying in accordance with data stored in a selected non-volatile memory cell, turns off the pre-charging circuit to drive the boosting capacitor, while applying a first potential to the drive terminal, to boost the potential at the sense node, and applies a retrieval voltage to a gate of the clamp transistor to transfer the data on the bit line to the sense node.

29. The non-volatile semiconductor device according to claim 28, wherein the sense amplifier circuit continuously lowers the retrieval voltage to a level higher than a threshold level of the clamp transistor and then stops boosting the sense node by applying a second potential to the drive terminal of the boosting capacitor, the second potential being lower than the first potential.

30. The non-volatile semiconductor device according to claim 19, the non-volatile memory cells are electrically erasable programmable non-volatile memory cells.

31. The non-volatile semiconductor device according to claim 26, the non-volatile memory cells are electrically erasable programmable non-volatile memory cells.

32. The non-volatile semiconductor device according to claim 27, the non-volatile memory cells are electrically erasable programmable non-volatile memory cells.